REMARKS

Claims 1-20 are in the application. The allowable subject matter of claims 5-8, 13, 14, and 16-18 is noted.

By this amendment, claims 2, 4, 11, 12, and 17-20 have been amended to more particularly set out applicant's invention. Paragraphs [0018] and [0021] together with FIG. 1 support the claim amendments. Additionally, the specification has been amended to address several minor typographical errors.

Claims 1-4, 9-12, 15, 19 and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by Lotfi et al., U.S. Publication No. U.S. 2001/0050393A1 ("Lotfi"). This rejection is respectively traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 1 calls for a dc/dc converter comprising an inductor coupled to one of a positive output terminal and a positive input terminal. A first depletion mode compound semiconductor FET is coupled to the inductor. A control circuit is coupled to the first depletion mode compound semiconductor FET. A capacitor is coupled to the positive output terminal and a negative terminal.

Applicant respectively submits that Lotfi fails to anticipate claim 1 because Lotfi does not teach a depletion mode compound semiconductor FET. Specifically, Lotfi states at paragraph [0032] that the characteristics of his device are such that it is "normally-off," and that a positive bias is required to turn his device on. As shown in the attached tables from S.M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, pgs. 323 and 454 (1981), normally off devices are enhancement mode devices. Since Lotfi does not teach a

depletion mode or normally on device as claimed, applicants respectfully submit that Lotfi fails to anticipate claim 1.

Claim 2 depends from claim 1 and further calls for the first depletion mode compound semiconductor FET to comprise a GaAs n-channel depletion mode JFET. Claim 2 is believed allowable for the same reasons as claim 1. Additionally, claim 2 is believed allowed because Lotfi does not teach a GaAs n-channel depletion mode JFET. In particular, Lotfi teaches an enhancement mode MOSFET as described in paragraph [0032] and FIGS. 3-5.

Claim 3 depends from claim 1 and is believed allowable for at least the same reasons as claim 1.

Claim 4 depends from claim 3 and further calls for the second depletion mode compound semiconductor FET to comprise a GaAs n-channel depletion mode JFET. Claim 4 is believed allowable for the same reasons as claims 3 and 1. Additionally, applicant respectfully submits that claim 4 is allowable because Lotfi does not show a second GaAs n-channel depletion mode JFET. As stated above, Lotfi teaches an enhancement mode MOSFET.

Claims 9 and 10 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 11 depends from claim 10 and further calls for one of the first and the second depletion mode compound semiconductor FETs to comprise a GaAs n-channel depletion mode JFET. Claim 11 is believed allowable for the same reasons as claims 10 and 1. Additionally, applicant respectfully submits that claim 11 is allowable because Lotfi does not teach a first and second depletion mode compound semiconductor FETS where one is a GaAs n-channel depletion mode JFET.

Claim 12 depends from claim 10 and further calls for both the first and second depletion mode compound semiconductor FETS to comprise GaAs n-channel depletion mode JFETS. Claim 12 is believed allowable for at least the same reasons as claims 10 and 1. Additionally, applicant respectfully submits that Lotfi does not teach first and second depletion mode compound semiconductor FETS that comprise GaAs n-channel depletion mode JFETS.

Claim 15 calls for a dc/dc converter network comprising a first vertical trench compound semiconductor depletion mode FET device. An inductor is connected to the first FET device and one of a positive input terminal and a positive output terminal. A gate control device is connected to the first FET device. A capacitor is connected to the positive output terminal.

Applicant respectfully submits that Lotfi fails to anticipate claim 15 for at least the following reasons. First, as described above in response to the rejection of claim 1, Lotfi does not teach a depletion mode device, but instead teaches an enhancement mode or normally off device as described in Lotfi's paragraph [0032]. Additionally, Lotfi does not teach a vertical device, but rather specifically teaches a lateral device as described in paragraph [0007] and FIGS. 3-5. Further, Lotfi does not teach a trench device, but rather teaches a planar device. Moreover, the Office Action states on page 3 that the prior art of record does not teach a "vertical trench compound semiconductor depletion mode FET." Applicant respectfully submits that this element is included in claim 15.

Claim 19 calls for a dc/dc converter circuit including an inductor connected to one of a positive input terminal and a positive output terminal. A first GaAs depletion mode

vertical JFET device is connected to the inductor. A second GaAs depletion mode vertical JFET device is connected to the first JFET device and a negative terminal. A gate control device is connected to the first and second JFET devices. A capacitor is connected to the positive output terminal and the negative terminal.

Applicant respectfully submits that Lotfi fails to anticipate claim 19 because Lotfi does not show a first or second GaAs depletion mode vertical JFET device. Rather, Lotfi shows an enhancement mode MOSFET device as described in paragraph [0032] and shown in FIGS. 3-5. Additionally, Lotfi does not teach a vertical device, but rather teaches a lateral device as described in paragraph [0007].

Claim 20 depends from claim 19 and is believed allowable for at least the same reasons as claim 19.

In view of all of the above, it is believed that the claims are allowable, and the case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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